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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/360,472	07/23/1999	RETO STAMM	X-528-US	4229

24309 7590 10/06/2003

XILINX, INC  
ATTN: LEGAL DEPARTMENT  
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SAN JOSE, CA 95124

EXAMINER

PHAN, THAI Q

ART UNIT PAPER NUMBER

2123

DATE MAILED: 10/06/2003

15

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.  
09/360,472

Applicant(s)  
Stamm et al.

Examiner  
Thai Phan

Art Unit  
2123



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Jul 18, 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_ 6) ☐ Other:

### DETAILED ACTION

This Office action is in response to applicants' amendment filed on July 18, 2003.

Claims 1-20 are pending.

### *Drawings*

1. The drawings filed on Oct. 25, 1999 are accepted.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goslin et al., US patent no. 6,120,549, in view of Kim et al., US patent no. 6,553,531 B1.

As per claim 1, Goslin discloses method and apparatus for design and verification of integrated circuit with feature limitations substantially similar to the claimed invention.

According to Goslin, the hardware design and verification includes steps:

parameterizing circuit functional blocks or logic circuit cores to meet user' specific requirement (col. 3, line 17 to col. 5, line 40),

generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed. Goslin does not especially disclose randomly generating a set of values for the logic core. Such claimed feature is however well known in the art. In fact, Kim teaches method and system for simulating integrated circuit design. Kim teaches parameter values of the design logic circuits are randomly generated for testing and verification such that the design testing and verification (col. 2, lines 52-57, col. 3, lines 37-50, col. 5, lines 42-53, for example) would be faster and accurate.

This would motivate practitioner in the art at the time of the invention was made to combine Kim teaching of random value generation of design variables in the design test and verification such as in Goslin parameterized logic cores in order to carry out a faster and accurate test and verification of the design as taught in Kim.

As per claim 2, Goslin teaches upper and lower limits associated with random parameter values (col. 6, lines 48-62, for example), and generating a new random parameter set for the design to meet design specification (col. 7, line 52 to col. 8, line 10).

As per claim 3, Goslin teaches weight file or probability function for parameter values generation in order to randomly generating parameter values (col. 9, line 20 to col. 10, line 14).

As per claim 4, Goslin teaches generating parameter values as input to a graphical user interface (col. 4, lines 26-43, col. 6, line 48 to col. 7, line 25), and replacement values for invalid parameter values to meet design requirement (col. 8, lines 15-60).

As per claim 5, Goslin teaches graphical user interface with feature limitations as claimed to allow user interactive with the design process (cols. 6-8).

As per claims 6 and 7, Goslin teaches generating replacement parameter values for the invalid parameters (col. 8, lines 15-60), and repeating such step for all parameters to meet design requirement.

As per claims 8-9, Goslin teaches parameters fitting and selection as in col. 8, lines 15-60, col. 9, lines 20-51, and col. 10, lines 25-40 could imply the claimed limitations of parameter mutation and cloning for optimizing the circuit verification performance because the fitting and parameter selection could require cloning and mutation as known for those skilled in the art to best fit parameter selection.

As per claim 10, in addition to fitting and selecting parameters for the design verification, Goslin also teaches generating a netlist for the new select set of parameter and simulation of the new netlist as claimed (col. 8, lines 4-10, and lines 15-60, and col. 9, lines 20-51).

As per claims 11-14, Goslin teaches design parameters selection and fitting which would obviously imply the claimed limitations in order to improve performance verification (col. 9, lines 20-51, col. 10, lines 25-40).

As per claim 15, Goslin teaches graphic user interface and interactive means to allow user to key in design parameters selection, change, or set as claimed (col. 4, lines 26-43, col. 6, line 48 to col. 7, line 25).

As per claim 16, Goslin teaches design order in order to generating parameters for the design, and generating parameter values for the orderly hierarchy of the design process (col. 5, lines 23-65, col. 6, lines 1-18, for example).

As per claim 17, Goslin teaches design verification including performance a number of design simulation, accumulating of fail test data, recording parameters of the design simulation, etc. in order to verify the design performance.

As per claim 18, Goslin discloses method and apparatus for design and verification of integrated circuit with feature limitations substantially similar to the claimed invention.

According to Goslin, the hardware design and verification includes steps:

parameterizing circuit functional blocks or logic circuit cores to meet user' specific requirement (col. 3, line 17 to col. 5, line 40),

generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed.

Goslin does not expressly disclose randomly generating a set of values for the logic core. Such claimed feature is however well known in the art. In fact, Kim teaches method and system for simulating integrated circuit design. Kim teaches method of randomly generating parameter values for design logic core to faster and accurate verification of the design circuit (col. 2, lines 52-57, col. 3, lines 37-50, col. 5, lines 42-53, for example).

This would motivate practitioner in the art at the time of the invention was made to combine Kim teaching of random value generation of design variables such as Goslin

parameterized logic cores in order to faster and accurately test and verify the design as taught in Kim above.

As per claim 19, Goslin discloses method and apparatus for design and verification of integrated circuit with feature limitations substantially similar to the claimed invention.

According to Goslin, the hardware design and verification includes steps:

parameterizing circuit functional blocks or logic circuit cores to meet user' specific requirement (col. 3, line 17 to col. 5, line 40),

generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed. Goslin does not expressly disclose randomly generating a set of values for the logic core. Such claimed feature is however well known in the art. In fact, Kim teaches method and system for simulating integrated circuit design. The method requires according to Kim teaches randomly generating parameter values for design logic core such that the design testing and verification will be faster and accurate (col. 2, lines 52-57, col. 3, lines 37-50, col. 5, lines 42-53, for example).

This would motivate practitioner in the art at the time of the invention was made to combine Kim teaching of random value generation of design variables such as Goslin parameterized logic cores in order to faster and accurately test and verify the design as taught in Kim above.

As per claim 20, Goslin discloses method and apparatus for design and verification of integrated circuit with feature limitations substantially similar to the claimed invention.

According to Goslin, the hardware design and verification includes steps:

parameterizing circuit functional blocks or logic circuit cores to meet user' specific requirement (col. 3, line 17 to col. 5, line 40),

generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed.

Goslin does not expressly disclose randomly generating a set of values for the logic core. Such claimed feature is however well known in the art. In fact, Kim teaches method and system for simulating integrated circuit design. Kim teaches method of randomly generating parameter values for design logic core to faster and accurate verification of the design circuit (col. 2, lines 52-57, col. 3, lines 37-50, col. 5, lines 42-53, for example).

This would motivate practitioner in the art at the time of the invention was made to combine Kim teaching of random value generation of design variables such as Goslin parameterized logic cores in order to carry out a faster and accurate test and verification of the design as taught in Kim above.



***Response to Arguments***

4. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

**or faxed to:**

(703) 872-9306, (for formal communications intended for entry)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

September 30, 2003

*Thai Phan*  
Patent Examiner  
Thai Phan  
AU 2123